

REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-20 in the application. In a previous response, the Applicant amended Claims 11-15. In the present response, no claims have been amended, canceled or added. Thus, Claims 1-20 are currently pending in the application.

The Examiner has indicated that dependent Claims 2-4, 7-9 and 12-14 would be allowable if rewritten in independent form including all of the limitations of the base claims and intervening claims. (*See Examiner's Action*, page 3.) The Applicant also believes that the other pending claims are allowable. Accordingly, the Applicant traverses the Examiner's rejection of Claims 1, 5-6, 10-11 and 15.

I. Rejection of Claims 1, 5-6, 10-11 and 15 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 5-6, 10-11 and 15 under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 5,857,005 to Ishibashi, *et al.* The Applicant respectfully disagrees since Ishibashi does not teach synchronizing an event signal from a first clock zone device to a second clock rate based upon an edge transition of the event signal and the second clock rate, and generate a synchronous notification signal therefrom as recited in independent Claims 1, 6 and 11.

Ishibashi is directed to an optical disk drive apparatus usable for optimizing the focusing position of an optical pickup with respect to an information recording surface of an optical disk medium. (*See column 1, lines 8-11.*) Ishibashi discloses an optical disk drive apparatus including a clock generator 300, a buffer memory 302, a memory controller 303 and a clock synchronizer 304. (*See column 10, line 66 to column 11, line 1 and Figure 8.*) The clock synchronizer 304 generates a write clock CKW that is synchronized with a digitized write data WD written into the buffer

memory 302. A read data RD is read from the buffer memory 302 and is synchronized with a read clock CKR generated by the clock generator 300. The frequency of the write clock CKW may differ from the frequency of the read clock CKR. (See column 11, lines 24-30 and Figure 8.)

Since the memory capacity of the buffer memory 302 is limited, the buffer memory 302 may overflow if the read-out rate of the data is higher than the write-in rate of the data. Therefore, when the remaining capacity of the buffer memory 302 becomes small, the memory controller 303 turns the write enable EW from "H" into "L", thereby prohibiting the write operation. (See column 11, lines 31-39.)

Ishibashi does not teach synchronizing an event signal from a first clock zone device to a second clock rate as recited in Claims 1, 6 and 11. On the contrary, even assuming the write clock CKW is an event signal, Ishibashi does not synchronize the CKW to the clock rate of the clock generator 300. Instead, to prevent overflow of the buffer due to different write and read speeds, Ishibashi prohibits writing to the buffer by setting the write enable EW to low. (See column 11, lines 32-39.) The Applicants do not find where the CKW is synchronized with the clock rate of the clock generator 300 or any other teachings of synchronizing an event signal from a first clock zone device to a second clock rate.

Therefore, Ishibashi does not disclose each and every element of independent Claims 1, 6 and 11 and Claims dependent thereon. Accordingly, Ishibashi does not anticipate Claims 1, 5-6, 10-11, and 15. The Applicant, therefore, respectfully requests the Examiner to withdraw the §102(a) rejection with respect to these Claims 1, 5-6, 10-11, and 15 and allow issuance thereof.

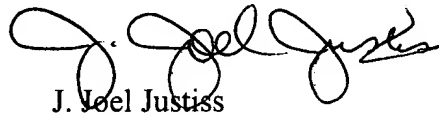
II. Conclusion

In view of the foregoing remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for all of the pending Claims 1-20.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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